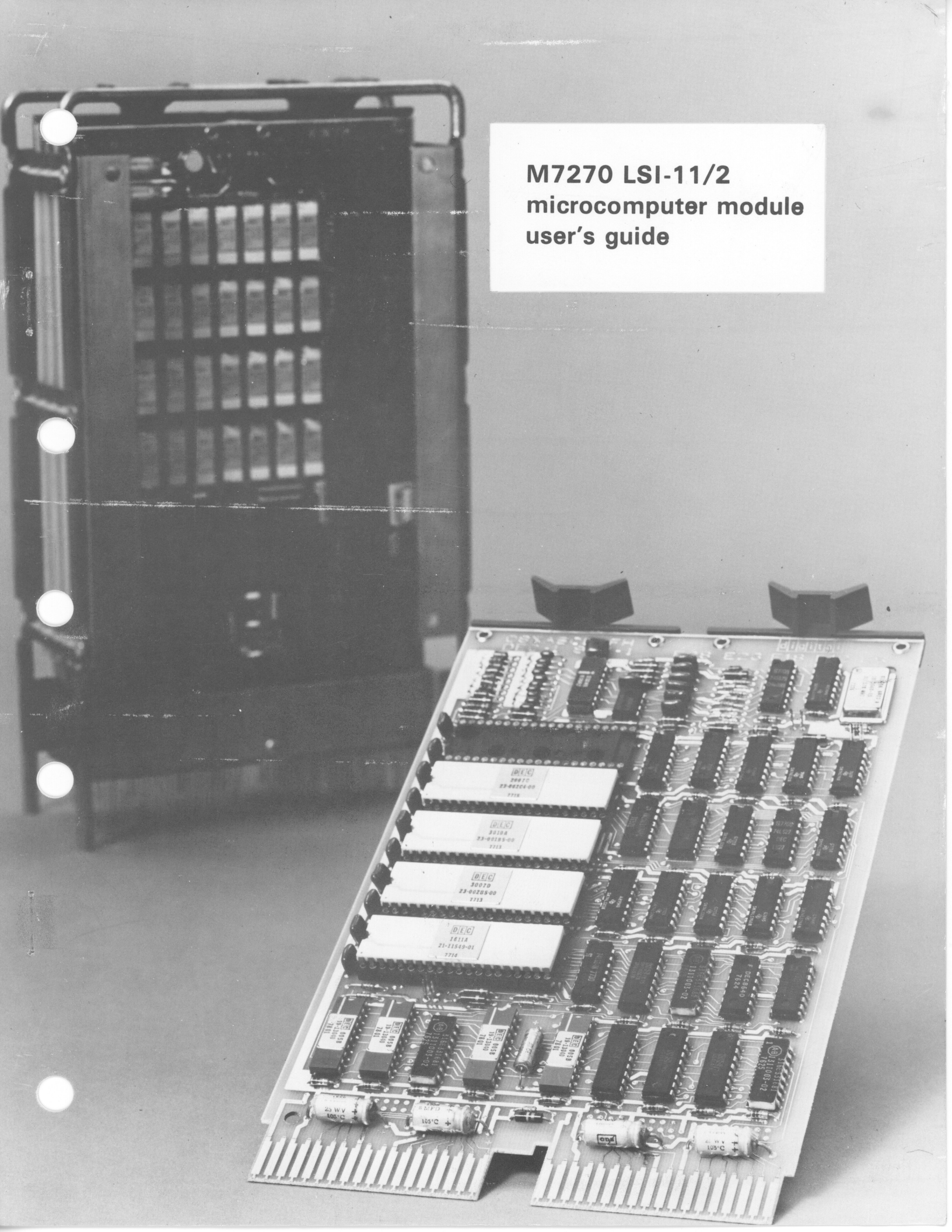
M7270 LSI-11/2 microcomputer module user's guide



M7270 LSI-11/2 microcomputer module user's guide

EK-LSI11-UG-001

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CHAPTER 1
INTRODUCTION

1.1 GENERAL

This manual contains specifications, installation procedures, a technical description, and user maintenance information for the KD11-HA (M7270) LSI-11/2 processor module (Figure 1-1). The M7270 processor module provides all the instructions, addressing modes, and LSI-11 bus compatibility available in the LSI-11 microcomputers described in the *Microcomputer Handbook*. However, the M7270 processor module contains no on-board (resident) memory, and does not generate memory refresh bus signals. The M7270 includes an additional circuit that self-initializes the system in which it is installed when operating power is applied.

The logic circuits that comprise the M7270 are similar to those contained on other LSI-11 processor modules. Specific differences are described in Chapter 3.

LSI-11 processor options in which the M7270 is included are listed below.

Option No.	Module(s)	Description
KD11-HA	M7270	Processor module only (no memory)
KD11-HB	M7270, M8044-BA	Processor module plus 8K × 16-bit read/write memory module
KD11-HC	M7270, M8044-CA	Processor module plus 16K × 16-bit read/write memory module
KD11-HD	M7270, M8044-DA	Processor module plus 32K × 16-bit read/write memory module
KD11-HF	M7270, M8044-AA	Processor module plus 4K × 16-bit read/write memory module
KD11-HU	M7270, M8021	Processor module plus 4K ultraviolet erasable programmable read-only memory (UV PROM) – 256-word read/write memory module. Memory module is supplied without UV PROM integrated circuits. Sockets are mounted on the module for user installation of PROM integrated circuits (type MRV11-BC). (Refer to the description for the MRV11-BA UV PROM/RAM module in the *Microcomputer Handbook.)*

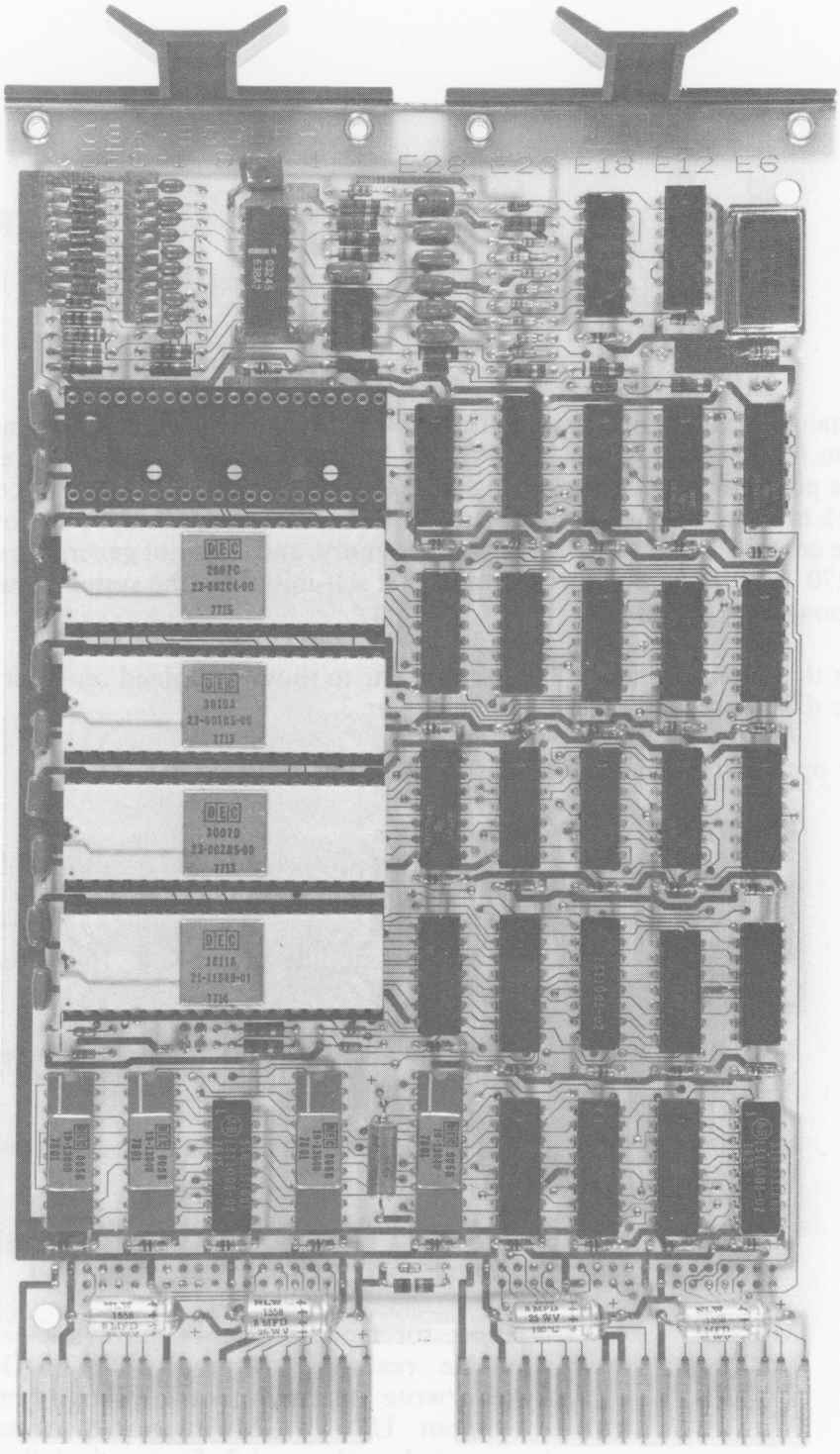

Figure 1-1 KD11-HA (M7270) LSI-11/2 Processor Module

Each LSI-11/2 processor features the following.

- A low-cost, powerful processor for integration into any small- or medium-sized computer system
- Direct addressing of 32K 16-bit words or 64K 8-bit bytes (K = 1024)
- Efficient processing of 8-bit characters without the need to rotate, swap, or mask
- Asynchronous operation that allows system components to run at their highest possible speed; replacement with faster devices means faster operation without other hardware or software changes.
- A modular component design that provides ease and flexibility in configuring systems
- Hardware memory stack for handling structured data, subroutines, and interrupts
- Direct-memory access for high-data-rate devices inherent in the bus architecture
- Eight general-purpose registers that are available for data storage, pointers, and accumulators; two are dedicated: SP and PC.
- LSI-11 bus structure that provides position-dependent priority as peripheral device interfaces are connected to the I/O bus
- Fast interrupt response without device polling
- A powerful and convenient set of programming instructions
- A jumper-selected power-up mode that enables restart through a power-up vector, console On-Line Debugging Technique (ODT) microcode subset, or a bootstrap program contained on a separate hardware option
- An ODT microprogram that controls all manual entry/display functions previously performed by a control panel through a serial ASCII device (optional) which is capable of transmitting and receiving ODT commands and data
- Compact size – only 22.8 by 13.2 cm (8.9 by 5.2 in)

1.2 SPECIFICATIONS

1.2.1 Physical

Height:	13.2 cm (5.2 in)
Length:	22.8 cm (8.9 in)
Width:	1.27 cm (0.5 in)
Weight:	213 g (7.5 oz)

1.2.2 Power Requirements

+5 V ± 5 percent, 1.2 A
+12 V ± 3 percent, 0.22 A

1.2.3 Backplane Pin Utilization

Backplane pin connections for the M7270 module are listed in Table 1-1. The table also includes pin utilization and signal names unique to the M7270 module and a list of standard LSI-11 bus backplane names associated with each pin. Note that although signal names may differ, the module is completely LSI-11 bus compatible.

Table 1-1 M7270 Module Backplane Pin Utilization

Side 1 (Component Side)

Backplane Pin	M7270 Signal Function	LSI-11 Bus Signal Name
AA1	Bus terminator	BIRQ5 L
AB1	Bus terminator	BIRQ6 L
AC1	Bus terminator	BDAL16 L
AD1	Bus terminator	BDAL17 L
AE1	STOP L	SSPARE1
AF1	SRUN L	SSPARE2
AH1	SRUN L	SSPARE3
AJ1	GND	GND
AK1	MTOE L	MSPAREA
AL1	GND	MSPAREA
AM1	GND	GND
AN1	BDMR L	BDMR L
AP1	BHALT L	BHALT L
AR1	Bus terminator	BREF L
AS1	Not Connected	+12B
AT1	GND	GND
AU1	Not Connected	PSPARE1
AV1	Not Connected	+5B
BA1	BDCOK H	BDCOK H
BB1	BPOK H	BPOK H
BC1	SCLK3 H	SSPARE4
BD1	SWMIB18 H	SSPARE5
BE1	SWMIB19 H	SSPARE6
BF1	SWMIB20 H	SSPARE7
BH1	SWMIB21 H	SSPARE8
BJ1	GND	
BK1	Not Connected	MSPAREB
BL1	Not Connected	MSPAREB
BM1	GND	
BN1	BSACK L	BSACK L
BPI	Bus terminator	BIRQ7 L
BR1	BEVNT L	BEVNT L
BS1	Not connected	+12B
BT1	GND	GND
BU1	Not connected	PSPARE2
BV1	+5 V	+5 V

Table 1-1 M7270 Module Backplane Pin Utilization (Cont)

Side 2 (Solder Side)

Backplane Pin	M7270 Signal Function	LSI-11 Bus Signal Name
AA2	+5 V	+5 V
AB2	Not connected	−12 V
AC2	GND	GND
AD2	+12 V	+12 V
AE2	BDOUT L	BDOUT L
AF2	BRPLY L	BRPLY L
AH2	BDIN L	BDIN L
AJ2	BSYNC L	BSYNC L
AK2	BWTBT L	BWTBT L
AL2	BIRQ L	BIRQ L
AM2	Not connected	BIAKI L
AN2	BIAKO L	BIAKO L
AP2	BBS7 L	BBS7 L
AR2	Not connected	BDMGI L
AS2	BDMGO L	BDMGO L
AT2	BINIT L	BINIT L
AU2	BDAL0 L	BDAL0 L
AV2	BDAL1 L	BDAL1 L
BA2	+5 V	+5 V
BB2	Not connected	−12 V
BC2	GND	GND
BD2	+12 V	+12 V
BE2	BDAL2 L	BDAL2 L
BF2	BDAL3 L	BDAL3 L
BH2	BDAL4 L	BDAL4 L
BJ2	BDAL5 L	BDAL5 L
BK2	BDAL6 L	BDAL6 L
BL2	BDAL7 L	BDAL7 L
BM2	BDAL8 L	BDAL8 L
BN2	BDAL9 L	BDAL9 L
BP2	BDAL10 L	BDAL10 L
BR2	BDAL11 L	BDAL11 L
BS2	BDAL12 L	BDAL12 L
BT2	BDAL13 L	BDAL13 L
BU2	BDAL14 L	BDAL14 L
BV2	BDAL15 L	BDAL15 L

1.2.4 Environmental

Operating	5° to 60° C (41° to 140° F) at altitudes below 2.4 km (8000 ft) with adequate airflow across the component surface of the module. Derate the maximum temperature by 1° C (1.8° F) for each 300 m (1000 ft) of altitude above 2.4 km (8000 ft). Relative humidity range is 10 to 90 percent (no condensation). Adequate airflow must be provided to limit the inlet-to-outlet temperature rise across the module to 5° C (9° F) when the inlet temperature is 60° C (140° F). For operation below 55° C (131° F), airflow must be provided to limit the inlet-to-outlet temperature rise across the module to 10° C (18° F) maximum.
Storage	–40° to 66° C (–40° to 151° F) with a relative humidity of 10 to 90 percent (no condensation).

NOTE

Before operating a module that has been stored in an environment outside the specified operating environment, the module must be allowed to stabilize at the operating temperature for 5 minutes (minimum).

1.3 RELATED HARDWARE MANUALS

The primary hardware reference documents for the M7270 processor module include this manual (for configuring and installing the module) and the *Microcomputer Handbook* for general LSI-11 system information, including LSI-11 bus protocol, installation and technical details for various hardware options, processor instruction set and addressing modes, and operating instructions. Additional references include Appendix A of this manual for installing and using H9281 backplanes, and manuals that document memory modules included with the various M7270 options. A list of publications is provided below.

Title	Document No.	Notes
1977–1978 Microcomputer Handbook, second edition	EB-07948-53/77	Required reference for use with all M7270 options. Available on hard copy.
MSV11-D, -E User's Manual	EK-MSV1D-OP-001	Required reference for use with KD11-HB, HC, HD, and HF options. Available on hard copy.
MRV11-BA LSI-11 UV PROM-RAM User's Manual	EK-MRV11-TM-001	Optional reference for use with KD11-HU. Required information is contained in the *Microcomputer Handbook,* second edition. Available on hard copy.

These documents can be ordered from:

Digital Equipment Corporation
444 Whitney Street
Northboro, MA 01532

Attention: Communications Services (NR2/M15)
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CHAPTER 2
INSTALLATION

2.1 GENERAL

The procedure for installing the M7270 LSI-11/2 processor module is similar to the procedure described in the *Microcomputer Handbook* for other LSI-11 processors. Items that must be considered for processor installation include the following.

1. Install jumpers to select certain processor operational features.
2. Select and mount an LSI-11 bus-structured backplane (or backplanes) in which the LSI-11 system modules will be installed.
3. Determine which options (memory and peripheral devices) will be installed in the system, what is required for their operation, and where they should be installed.
4. Select and connect an appropriate power supply to the backplane.
5. Add bus accessory options as required or desired.

Each item is discussed in detail in the following paragraphs. Refer to the list of related documents in Paragraph 1.3 for detailed descriptions of specific options.

2.2 CONFIGURING PROCESSOR MODULE JUMPERS

2.2.1 General

Figure 2-1 shows the location of the four M7270 processor module jumpers. Each jumper-selected function is described in the following paragraphs.

NOTE

The M7270 processor module does not contain on-board memory. Hence, memory-related jumpers contained on other LSI-11 processor modules are not included on the M7270. Those jumpers include resident memory bank select (W1 and W2), processor-controlled memory refresh (W4), bias voltages (W7 and W8), resident memory reply (W9 and W10), and on-board memory select enable (W11).

2.2.2 W1 – Master Clock Enable

W1 must always be installed for processor operation. It is provided for manufacturing test purposes and normally should not be removed.

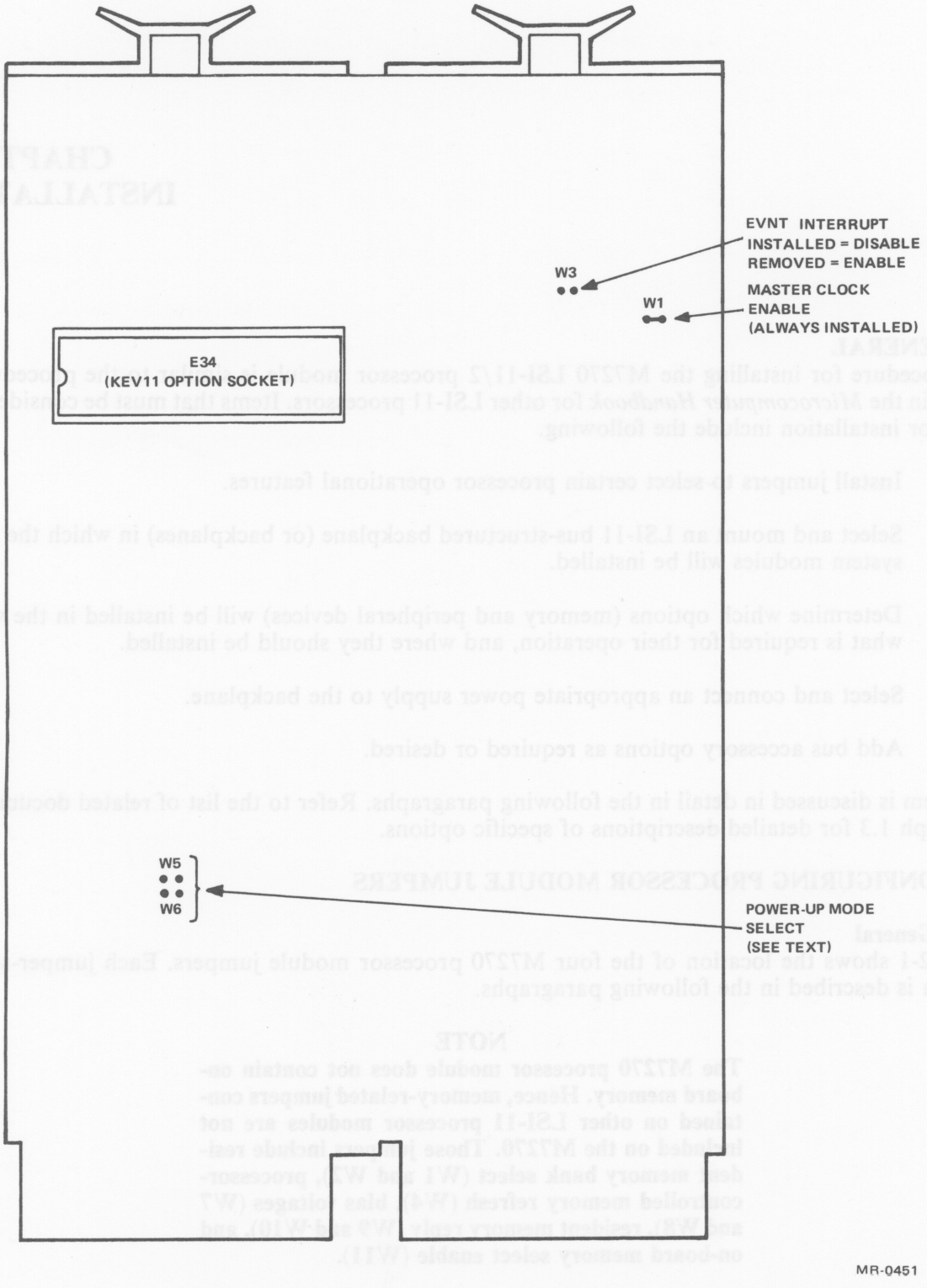


Figure 2-1 M7270 Jumpers and Socket Locations

2.2.3 LTC Interrupt

Line-time clock (LTC) or external event (EVNT) interrupts are enabled when jumper W3 is removed and the processor is running. The jumper can be inserted to disable this feature. The LTC interrupt is initiated by an external device when it asserts the BEVNT L signal. This is the highest priority external interrupt request; processor interrupts have higher priorities. If external interrupts are enabled (PS bit 7 = 0), the processor PC (R7) and PS word are pushed onto the processor's stack. The LTC (or external event device) service routine is entered by vector address 100; the usual interrupt vector address input operation by the processor is not required since vector 100 is generated by the processor.

The first instruction of the service routine typically will be fetched within 16 μs from the time BEVNT L is asserted; however, if optional EIS/FIS instructions are being executed, this time could extend to 44.1 μs maximum. This time could also be extended by processor trap execution (memory refresh, T-bit, power fail, etc.), or by asserting the BHALT L signal.

2.2.4 Power-Up Mode Selection

Four power-up modes are available for user selection. These are selected (or changed) by wire-wrap jumpers W5 and W6 on the processor module. Note that the jumpers affect only the power-up mode (after BDCOK H and BPOK H have been asserted); they do not affect the power-down sequence.

The state of the BHALT L signal is significant during the power-up sequence. When this signal is asserted, it invokes the processor's ODT console microcode after the power-up sequence has been completed. The console device must be properly installed for correct use of the BHALT L signal.

Power-up modes are listed below. Detailed descriptions of each mode are provided in the paragraphs that follow.

Mode	Jumpers*		Mode Selected
	W6	W5	
0	R	R	PC at 24 and PS at 26, or halt mode
1	R	I	ODT microcode
2	I	R	PC at 173000 for user bootstrap
3	I	I	Special processor microcode (not implemented)

* R = Jumper Removed; I = Jumper Installed.

Power-Up Mode 0

This option places the processor in a microcode sequence that fetches the contents of memory locations 24 and 26 and loads their contents into R7 and the PS, respectively. A microcode service translation at this point interrogates the state of the BHALT L signal. Depending on the state of this signal, the processor either enters ODT microcode (BHALT L asserted low) or begins program execution with the current contents of R7 as the starting address (BHALT L not asserted).

Note that the T-bit (PS bit 4) is loaded with the contents of PS bit 4 in location 26. This mode should be used only with nonvolatile memory (or volatile memory with battery backup) for locations 24 and 26, or with BHALT L asserted. This power-up sequence is shown in Figure 2-2.

Power-Up Mode 1

This mode immediately places the processor in the console microcode regardless of the state of the BHALT L signal. This mode assumes a console interface device at bus address 177560.

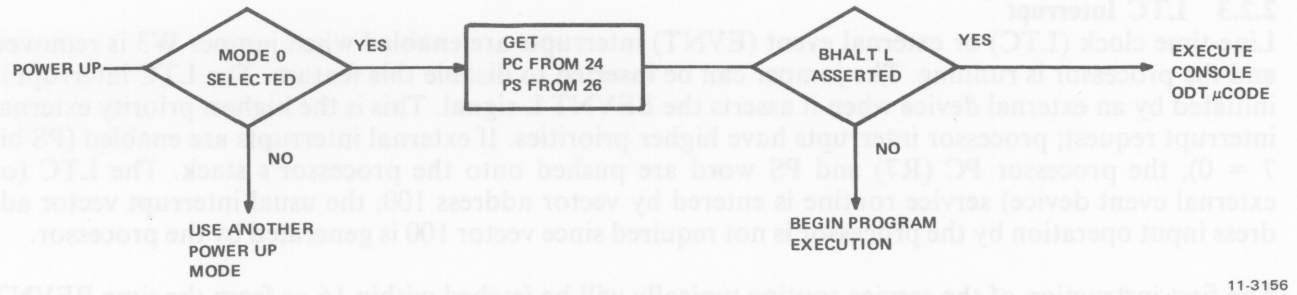


Figure 2-2 Mode 0 Power-Up Sequence

Power-Up Mode 2

This mode places the processor in a microcode sequence that loads a starting address of 173000 into R7 and begins program execution at this location if the BHALT L signal is not asserted.

Note that before 173000 is loaded into R7, PS bit 4 (T-bit) is cleared and bit 7 (interrupt disable) is set. The user's program must set these bits, as desired, and set up a valid stack pointer (R6). This option should be used with nonvolatile memory (ROM, PROM, or core) at address 173000. A time-out trap through location 4 will occur if no device exists at location 173000.

This mode is particularly useful when an REV11 option is present in the system. Useful power-up, diagnostic, and bootstrap routines are implemented in PROMs contained on the REV11 module. By selecting power-up mode 2, REV11 program execution is automatically started when the system is turned on.

If BHALT L is asserted, the processor will not execute the instruction at location 173000 and will immediately execute the console microcode. This power-up mode sequence is shown in Figure 2-3.

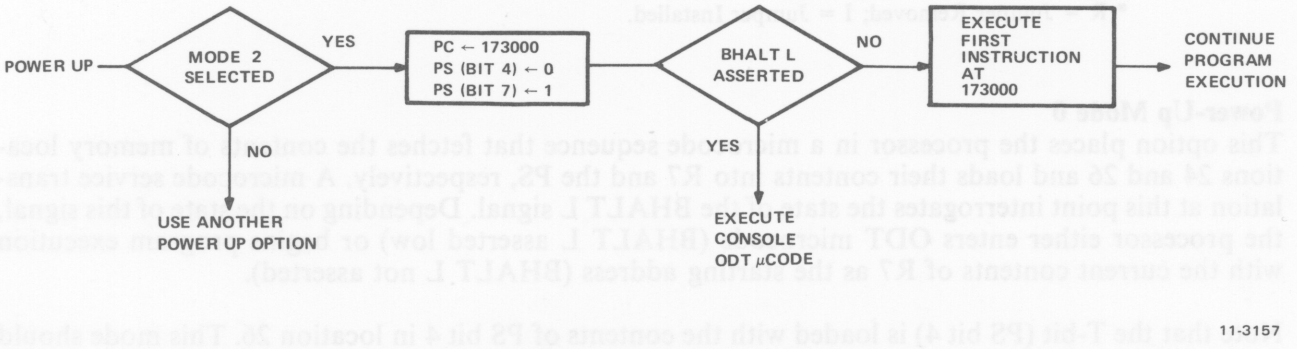


Figure 2-3 Mode 2 Power-Up Sequence

Power-Up Mode 3
This microcode sequence allows access to future microcode expansion in the fourth microm page (microlocations 3000 to 3777). After BDCOK H and BPOK H are asserted and the internal flags are cleared, a microjump is made to microlocation 3002. If this option is selected and no microm responds to the fourth page microaddress, a microtrap will occur through microlocation 0 which will, in turn, cause a reserved user instruction trap through location 10.

Note that the state of BHALT L is not checked before control is transferred to the fourth microm page.

2.3 INSTALLATION

2.3.1 General
When installing the M7270 processor module in a system, the following items must be considered.

1. System backplane
2. Memory modules used
3. Peripheral device priority
4. Peripheral device and memory options required

Each of the above items are discussed in the following paragraphs.

2.3.2 System Backplanes
LSI-11 systems using the M7270 processor module can be configured using the H9270 or DDV11-B backplanes described in the *Microcomputer Handbook,* or one of the newer H9281 "two-slot" backplanes can be used.

2.3.2.1 Using H9281 Backplanes – H9281 backplanes are designed to accept "double-height" modules only; double-height module dimensions are 13.2 cm (5.2 in) high, 22.8 cm (8.9 in) long, and 1.27 cm (0.5 in) wide. The M7270 processor module is a double-height module. The following lists present memory and peripheral device options that cannot be installed in a 2-slot backplane.

Option Designation	Module Number	Description
AAV11-A	A6001	4-channel 12-bit D/A converter
ADV11-A	A0121	16-channel 12-bit A/D converter
DRV11-B	M7950	DMA interface
DRV11-P	M7948	LSI-11 foundation module
MMV11-A	H223,G653	Core memory
MSV11-CD	M7955-YD	16K MOS memory
KWV11-A	M7952	Programmable line-time clock

If one or more of the above options are used, configure the system using the H9270 or DDV11-B backplane.

A list of H9281 2-slot backplane options is provided below. These backplanes allow the user to configure compact LSI-11 systems that most efficiently utilize available system space.

Backplane Option Designation	Description
H9281-AA	4-module LSI-11 backplane
H9281-AB	8-module LSI-11 backplane
H9281-AC	12-module LSI-11 backplane
H9281-BA	4-module LSI-11 backplane and card cage assembly
H9281-BB	8-module LSI-11 backplane and card cage assembly
H9281-BC	12-module LSI-11 backplane and card cage assembly

Mounting dimensions, processor and option locations, and electrical connections for H9281 series backplanes are shown in Appendix A.

2.3.2.2 Using H9270 and DDV11-B Backplane – H9270 and DDV11-B backplanes will accept the M7270 processor module in backplane location A1-B1. If the use of the processor's SRUN L signal is desired for driving a RUN indicator (part of the H780-H or J power supply console), it is necessary to install (wire wrap) a wire between backplace pins AF1 and the bus signal connector SRUN pin; this signal pin is located as shown in Figure A-4.

2.3.3 Peripheral Device Priority

Peripheral device priority when using the M7270 processor module on H9281 backplanes is described in Appendix A. Device priority is covered in detail for H9270 and DDV11-B backplanes in the *Microcomputer Handbook*. However, since two additional slots (one option location) are available when using the M7270 processor, the options move one location closer to the processor. Refer to Figures 2-4 and 2-5 for device priority on H9270 and DDV11-B backplanes, respectively.

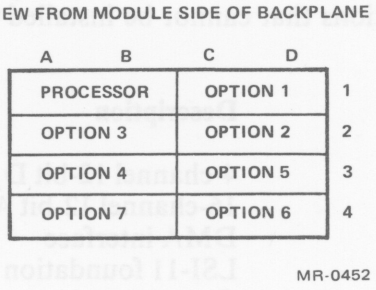


Figure 2-4 H9270 Option Priority

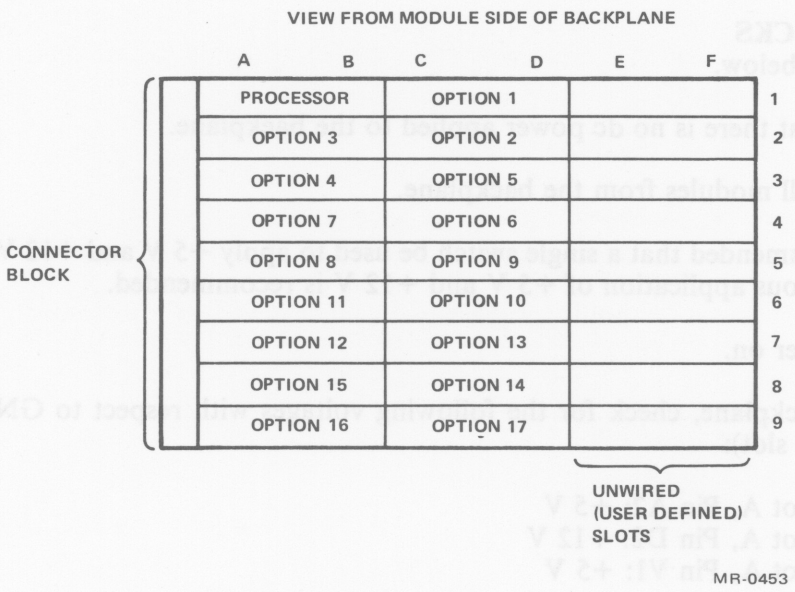


Figure 2-5 DDV11-B Option Priority

2.3.4 Memory Requirements

Each LSI-11 system must contain memory in "Bank 0" (addresses ranging from 0 through 17777). Specifically, memory location 000004 must respond to the processor during power-up. Either read-only or read-write memory may be used. The processor executes a "dummy read" cycle at this memory address and requires a reply. If the reply is not present, the processor continues to attempt to read the location as bus timeouts occur. Hence, the processor will appear to "hang."

If MSV11-B memory modules are installed in the system, memory refresh signals must be supplied. LSI-11 options that provide refresh signals include REV11-A and REV11-C DMA refresh/bootstrap modules. MSV11-CD and all MSV11-D memory options contain on-board memory refresh and do not require externally generated refresh signals.

2.3.5 Memory and Peripheral Devices Required

A minimum LSI-11 system includes the M7270 processor module, one or more memory modules, and a console terminal and interface module. If user programs are not contained in PROM (MRV11-AA, AC or MRV11-BA, BC options), it is necessary to include a means for loading user programs. An inexpensive means for loading paper tape programs can be obtained by using a PRS01 reader and a DLV11 serial line unit interface. Systems based on the M7270 processor can be configured upward to include 30K read/write and/or PROM memory, mass storage devices (RXV11 floppy disk or RKV11 disk systems), and various peripheral device interface modules and accessories. Refer to the *Microcomputer Handbook* and DEC sales literature for the latest list of LSI-11 options.

Diagnostic programs supplied by DEC are generally supplied on punched paper tape or disk. All disk-based systems, including floppy disks, require 8K (minimum) read/write memory. Paper tape diagnostics can generally be executed in systems containing as little as 4K read/write memory.

2.4 INITIAL CHECKS

Proceed as directed below.

1. Ensure that there is no dc power applied to the backplane.

2. Remove all modules from the backplane.

3. It is recommended that a single switch be used to apply +5 V and +12 V to the backplane. Simultaneous application of +5 V and +12 V is recommended.

4. Turn power on.

5. At the backplane, check for the following voltages with respect to GND (pin C2 in any backplane slot):

   Row 1, Slot A, Pin A2: +5 V
   Row 1, Slot A, Pin D2: +12 V
   Row 1, Slot A, Pin V1: +5 V

   CAUTION

   Do not plug in modules with power applied to backplane.

6. Turn power off.

7. Ensure that the system is properly configured and installed as previously described in Chapter 2 (M7270 processor module) and in the *Microcomputer Handbook,* Section 1, Chapters 5 and 6 (for other system modules).

8. Turn on system power. Observe that the console device responds as described in Table 2-1.

Table 2-1 Console Power-Up Printout (or Display)

Conditions	Mode 0 (W5, W6 removed)	Mode 1 (W6 removed, W5 installed)	Mode 2 (W6 installed, W5 removed)	Mode 3 (W5, W6 installed)
BHALT L (unasserted) Dynamic RAM Memory	Processor will execute program using contents of location 24 as the PC value.	Terminal will print out a random 6-digit number, which is the contents of the program counter.	Processor will execute program at location 173000. (See Note 2.)	No printout at terminal. (See Note 1.)
BHALT L (unasserted) Core or PROM Memory	Processor will execute program using contents of location 24 as the PC value.	Terminal will print out a random 6-digit number, which is the contents of the program counter.	Processor will execute program at location 173000. (See Note 2.)	No printout at terminal. (See Note 1.)
BHALT L (asserted) Dynamic RAM Memory	Terminal will print out contents of memory location 024 (normally "000000".)	Terminal will print out a random 6-digit number, which is the contents of the program counter.	Terminal will print out "173000."	No printout at terminal. (See Note 1.)
BHALT L (asserted) PROM or Core Memory	Terminal will print out contents of memory location 024 (normally "000000").	Terminal will print out a random 6-digit number, which is the contents of the program counter.	Terminal will print out "173000."	No printout at terminal. (See Note 1.)

NOTES

1. **If mode 3 is selected, and microaddress (3000–3777) is not implemented, the processor will trap to memory location 010 and start program execution using the contents of location 10 as the PC value and location 12 as the PSW value.**

2. **Normal mode for use with the REV11-A or REV11-C options. Normal display is a $ symbol, prompting the operator to input a command.**

CHAPTER 3
TECHNICAL DESCRIPTION

3.1 GENERAL

Basic functions that comprise the M7270 processor module are shown on Figure 3-1. These logic functions are similar to those described for other LSI-11 processor options in the *Microcomputer Handbook,* Section 1, Chapter 4. Functions added or changed are described in detail in the following paragraphs. Functions deleted include resident memory and memory refresh, as described in the *Microcomputer Handbook.*

3.2 DETAILED DESCRIPTION

3.2.1 Clock Pulse and Charge Pump Circuits

The clock pulse and charge pump circuits are shown on Figure 3-2. The clock pulse generator produces 4-phase clock signals for processor timing and synchronization and a 2.6 MHz clock pulse that drives the charge pump circuit.

The 4-phase clock generator outputs PH<1:4> L and PH<1:4> H synchronize TTL logic contained on the processor module. PH<1:4> L signals are also applied to MOS-compatible clock drivers that produce similarly timed +12 V RPH<1:4> H signals. These signals are used for driving the 4-phase clock inputs on the processor data, control, and microinstruction ROM integrated circuits. Each clock pulse phase signal is 95 ns duration and pulses occur at 380 ns intervals.

The charge pump is equivalent to the dc-dc inverter portion of the LSI-11 microcomputer module described in the *Microcomputer Handbook.* Outputs include VDVR (+13.4 V) voltage source for the MOS clock drivers and -VBB (-3.9 V) voltage bias for the processor data, control, and microinstruction ROM integrated circuits.

3.2.2 Wake-Up Circuit

The wake-up circuit (Figure 3-3) causes the LSI-11 processor to self-initialize during power-up. An R-C circuit receives +5 V operating power when power is turned on. When power is first applied, the low capacitor voltage causes the Schmitt trigger's output to go high and the bus driver asserts the BDCOK H signal (low). After power has been applied for approximately 1 second, the capacitor's voltage rises above the Schmitt trigger's threshold voltage, and its output goes low. The low voltage turns off the bus driver, enabling BDCOK H to become asserted. The processor then starts its initialization sequence if no other device is asserting BDCOK H. Proper initialization requires that +12 V operating power be applied before or simultaneously with +5 V operating power.

Normal operation of the wake-up circuit depends on the rise time of the +5 V power supply being faster than 50 ms. The +12 V power supply also must attain its specified operating voltage in the same 50 ms. The wake-up circuit does not provide power failure detection nor power-down sequencing. These functions, if required, must be generated externally.

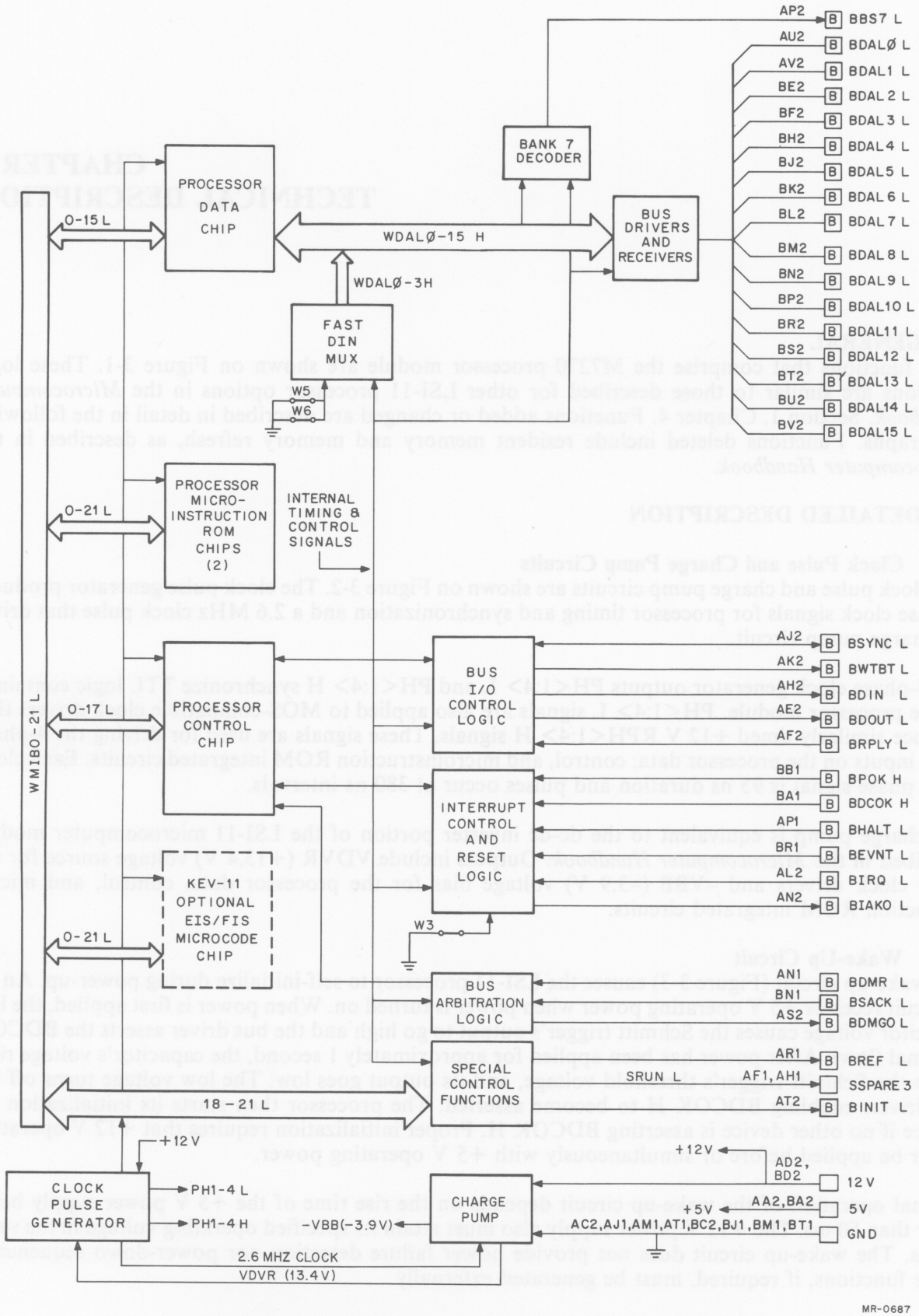


Figure 3-1 M7270 LSI-11/2 Processor Module-Basic Functions

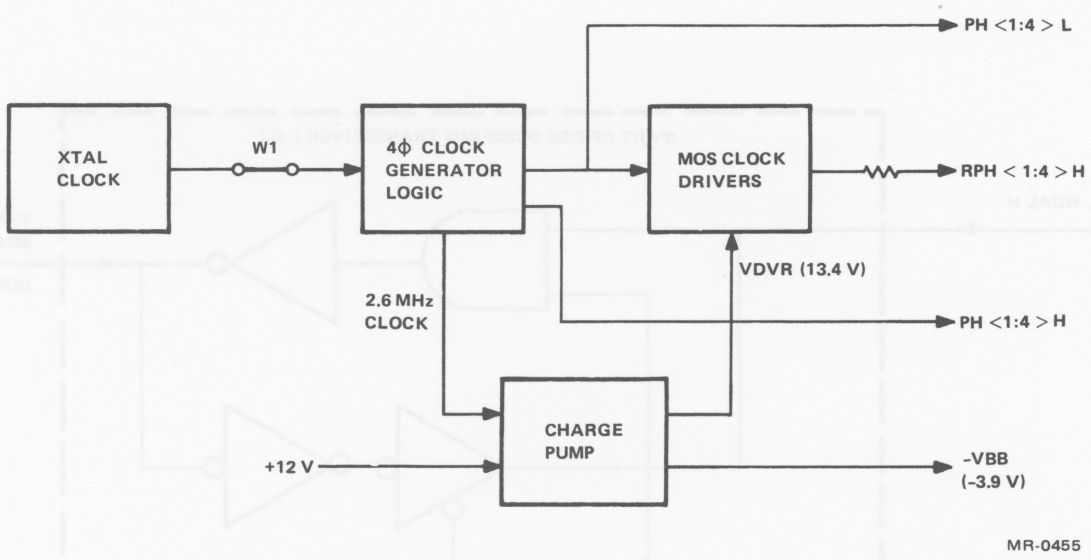


Figure 3-2 Clock Pulse and Charge Pump Circuits

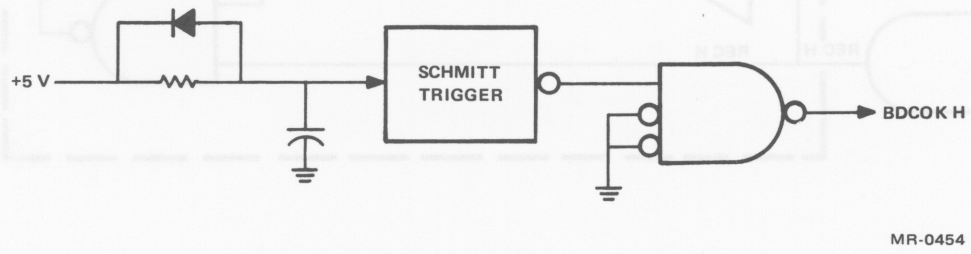


Figure 3-3 Wake-Up Circuit

3.2.3 BDAL Bus Driver Enable Logic

The EDAL L logic described in the *Microcomputer Handbook* is not used on the M7270 processor module. Instead, the logic circuit (Figure 3-4) is used. The four bus driver portions in each of four DEC DC005 bus transceiver integrated circuits are enabled whenever DMGCY(0) H is high (DMG cycle not in progress) and DIN H and FDIN(0) H are passive. The drivers are disabled whenever a DMG cycle is in progress, or when the processor is reading the bus [instruction fetch or data portion of DATI or DATIO(B) bus cycles]. Bus receivers are enabled only when FDIN(0) H and DIN H are both true (high).

3.2.4 DMA Arbitration Logic

The DMA arbitration logic circuit used on the M7270 processor is shown on Figure 3-5. Logic functions are synchronized by the trailing edge of the PH4 L clock signal. A typical DMA arbitration (DMA request/grant) sequence is shown on Figure 3-5.

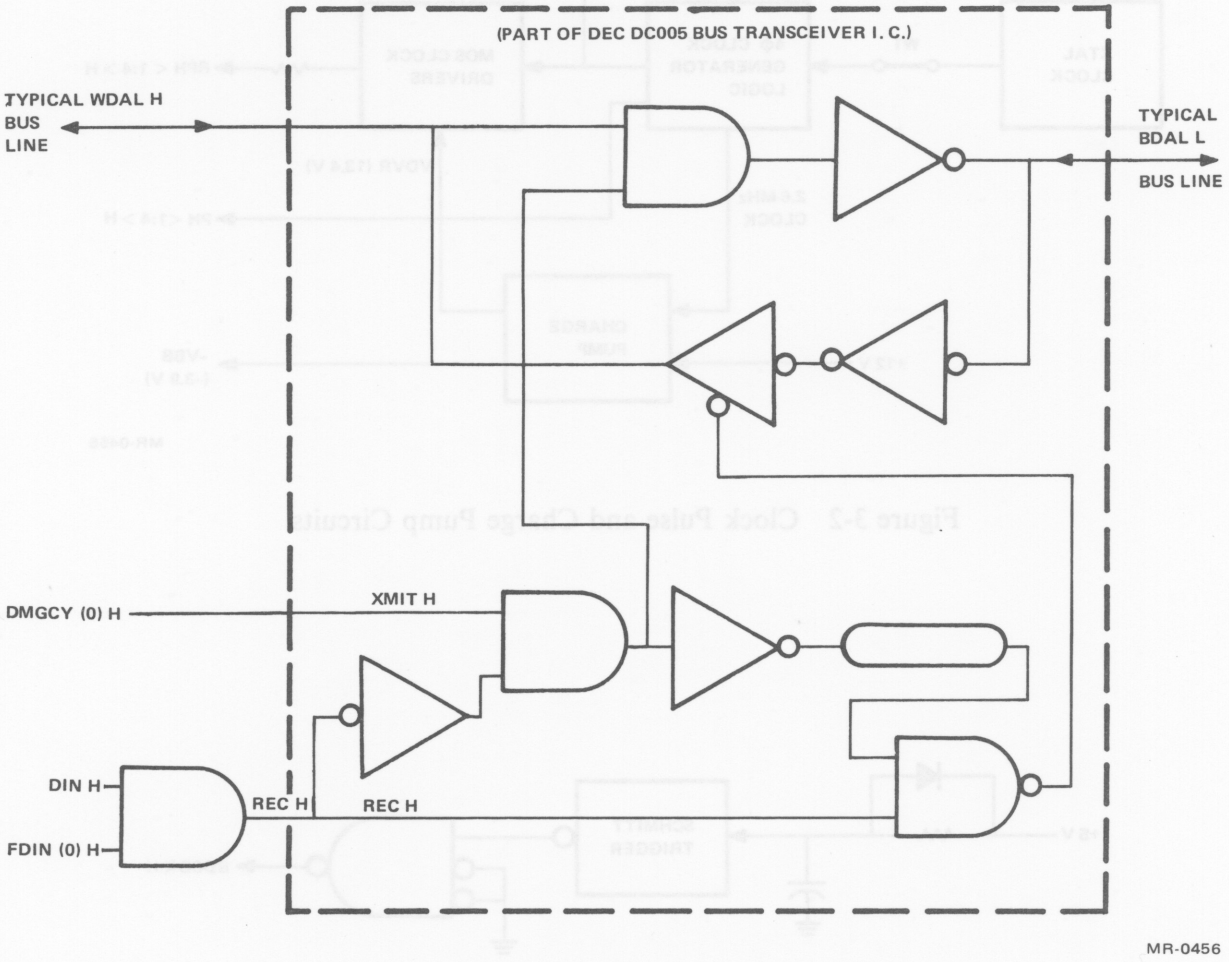


Figure 3-4 BDAL Bus Driver Enable Logic

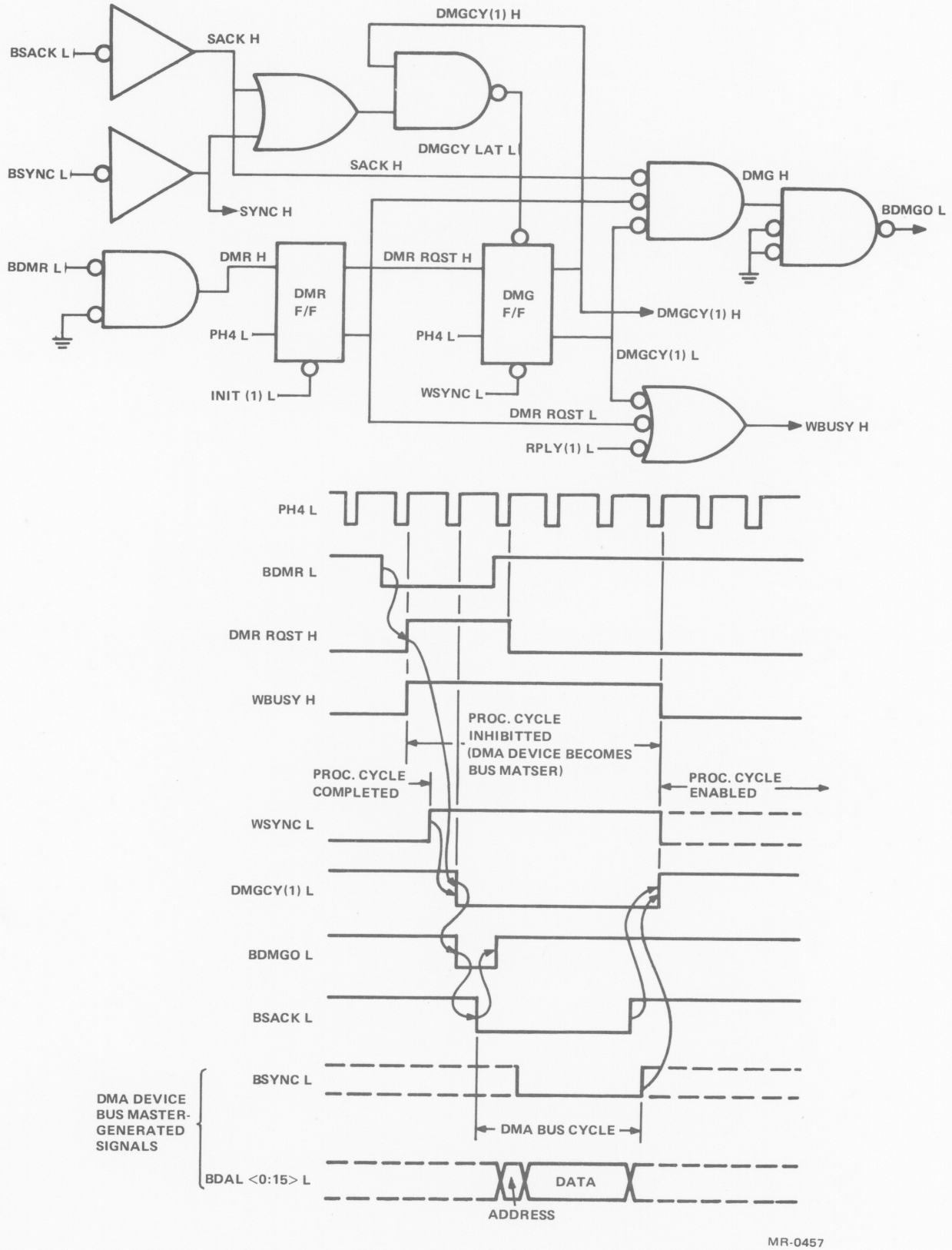


Figure 3-5 DMA Arbitration Logic and Sequence

CHAPTER 4
MAINTENANCE

4.1 GENERAL

Maintenance procedures required for the M7270 processor module are identical to those described in the *Microcomputer Handbook,* Section 1, Chapter 9, and Section 5, Chapter 3. Additional references are provided below.

4.2 INITIAL CHECKS

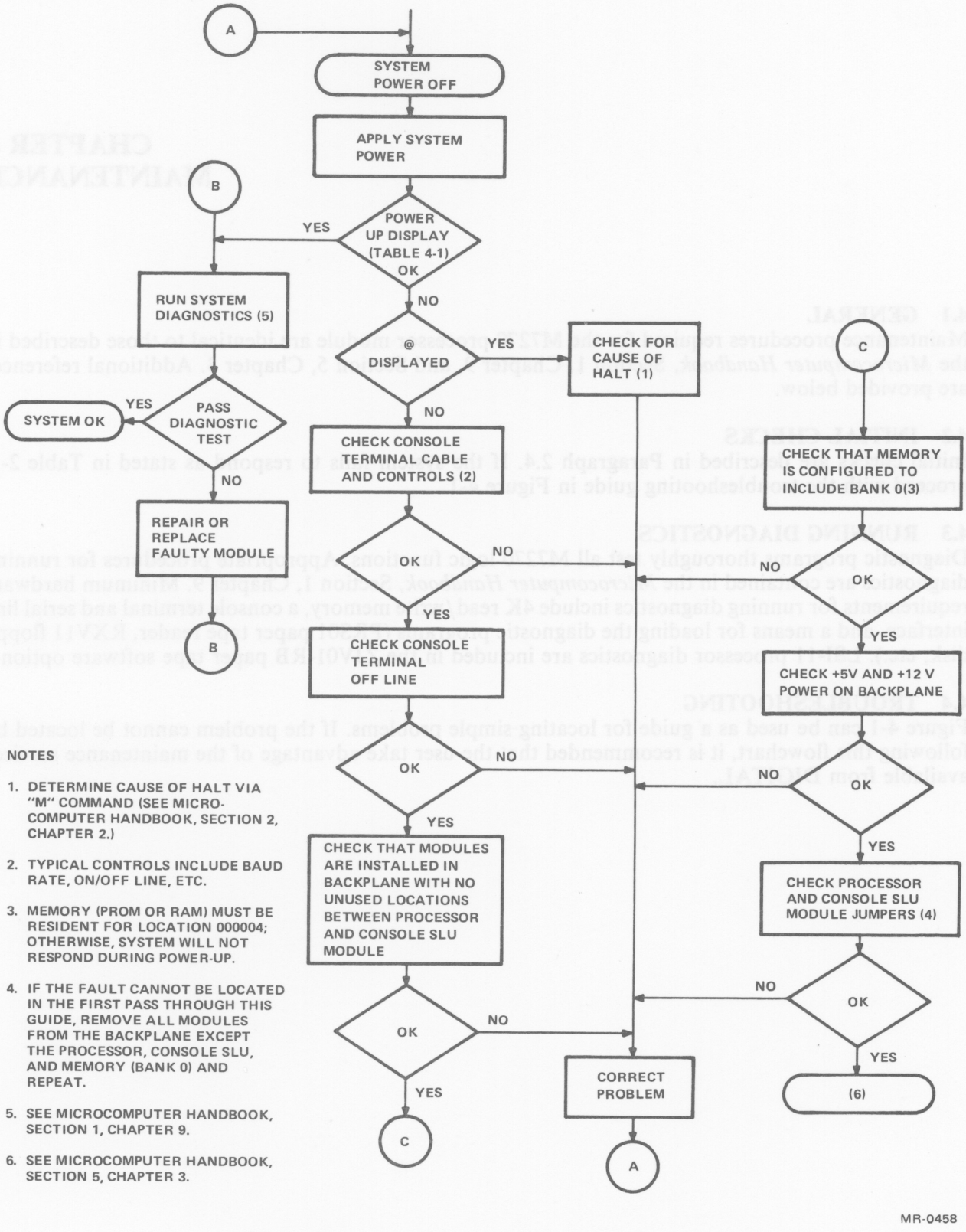
Initial checks are described in Paragraph 2.4. If the system fails to respond as stated in Table 2-1, proceed with the troubleshooting guide in Figure 4-1.

4.3 RUNNING DIAGNOSTICS

Diagnostic programs thoroughly test all M7270 logic functions. Appropriate procedures for running diagnostics are contained in the *Microcomputer Handbook,* Section 1, Chapter 9. Minimum hardware requirements for running diagnostics include 4K read/write memory, a console terminal and serial line interface, and a means for loading the diagnostic programs (PRS01 paper tape reader, RXV11 floppy disk, etc.). LSI-11 processor diagnostics are included in the ZJV01-RB paper tape software option.

4.4 TROUBLESHOOTING

Figure 4-1 can be used as a guide for locating simple problems. If the problem cannot be located by following this flowchart, it is recommended that the user take advantage of the maintenance services available from DIGITAL.



NOTES

1. DETERMINE CAUSE OF HALT VIA "M" COMMAND (SEE MICRO-COMPUTER HANDBOOK, SECTION 2, CHAPTER 2.)
2. TYPICAL CONTROLS INCLUDE BAUD RATE, ON/OFF LINE, ETC.
3. MEMORY (PROM OR RAM) MUST BE RESIDENT FOR LOCATION 000004; OTHERWISE, SYSTEM WILL NOT RESPOND DURING POWER-UP.
4. IF THE FAULT CANNOT BE LOCATED IN THE FIRST PASS THROUGH THIS GUIDE, REMOVE ALL MODULES FROM THE BACKPLANE EXCEPT THE PROCESSOR, CONSOLE SLU, AND MEMORY (BANK 0) AND REPEAT.
5. SEE MICROCOMPUTER HANDBOOK, SECTION 1, CHAPTER 9.
6. SEE MICROCOMPUTER HANDBOOK, SECTION 5, CHAPTER 3.

Figure 4-1 M7270 Troubleshooting Guide

APPENDIX A
H9281 BACKPLANE USER'S GUIDE

A.1 INSTALLATION

Mounting dimensions for H9281 backplanes are shown on Figures A-1 and A-2. Backplanes can be mounted in any plane. The enclosure in which the backplane is mounted, available system space, and cooling air flow will determine the backplane's position when installed in a particular system.

A.2 CONNECTING SYSTEM POWER

Seven screw terminals are provided on the "slot 1" end of the backplane for power connections. Connect system power (and optional battery backup power) as shown on Figure A-3. Power wiring should be done with a wire gauge appropriate for the total power requirements for options installed in the backplane. The recommended wire size for H9281-AC and BC backplanes is 12 gauge; 14 gauge is sufficient for other H9281 models.

Select a power supply that will meet LSI-11 system power specifications and supply sufficient current for the options comprising the system. The H780 power supply is recommended. It is capable of supplying +5 V ± 5 percent at up to 18 A and +12 V ± 3 percent at up to 3.5 A, 110 W (+5 V and +12 V total power) maximum. In addition, the H780 produces proper power-up/down sequencing signals. Technical descriptions, specifications, and installation details for the various H780 models are provided in the *Microcomputer Handbook*.

A.3 CONNECTING EXTERNALLY GENERATED BUS SIGNALS

Externally generated bus signals can be connected to the H9281 backplane via connector J2. These signals include power sequence signals BPOK H and BDCOK H, BHALT L and BEVNT L. In addition, the processor-generated SRUN L signal is available via J2 for driving a RUN indicator circuit. J2 connector pins are fully compatible with H9270 and DDV11-B LSI-11 backplanes and can be interfaced with standard DEC options such as the H780 model series power supply, or the KPV11-A power fail/line-time clock. Details for connecting the H780 or KPV11-A signals are provided in the *Microcomputer Handbook,* Section 1, Paragraphs 6.10 and 5.16, respectively. Externally generated bus signals for simple systems can be user-supplied as described in the *Microcomputer Handbook,* Section 1, Paragraph 6.7.6. Signal connector J2 pinning and signal names are identified on Figure A-4.

A.4 DEVICE PRIORITY

All LSI-11 backplanes are priority structured. Daisy-chained grant signals for DMA and interrupt requests propagate away from the processor to the first (highest priority device) to successively lower priority devices. Processor module location and device (option) priority are shown on Figure A-5.

A.5 BUS TERMINATIONS

Backplane models H9281-AB, BB, AC, and BC include 120 Ω bus termination resistors at the electrical end of the bus. It is not necessary to install a separate 120 Ω bus terminator module in these backplanes. These backplanes can be used unmodified for the minimum and intermediate configurations described in the *Microcomputer Handbook,* Section 1, Paragraph 3.13.

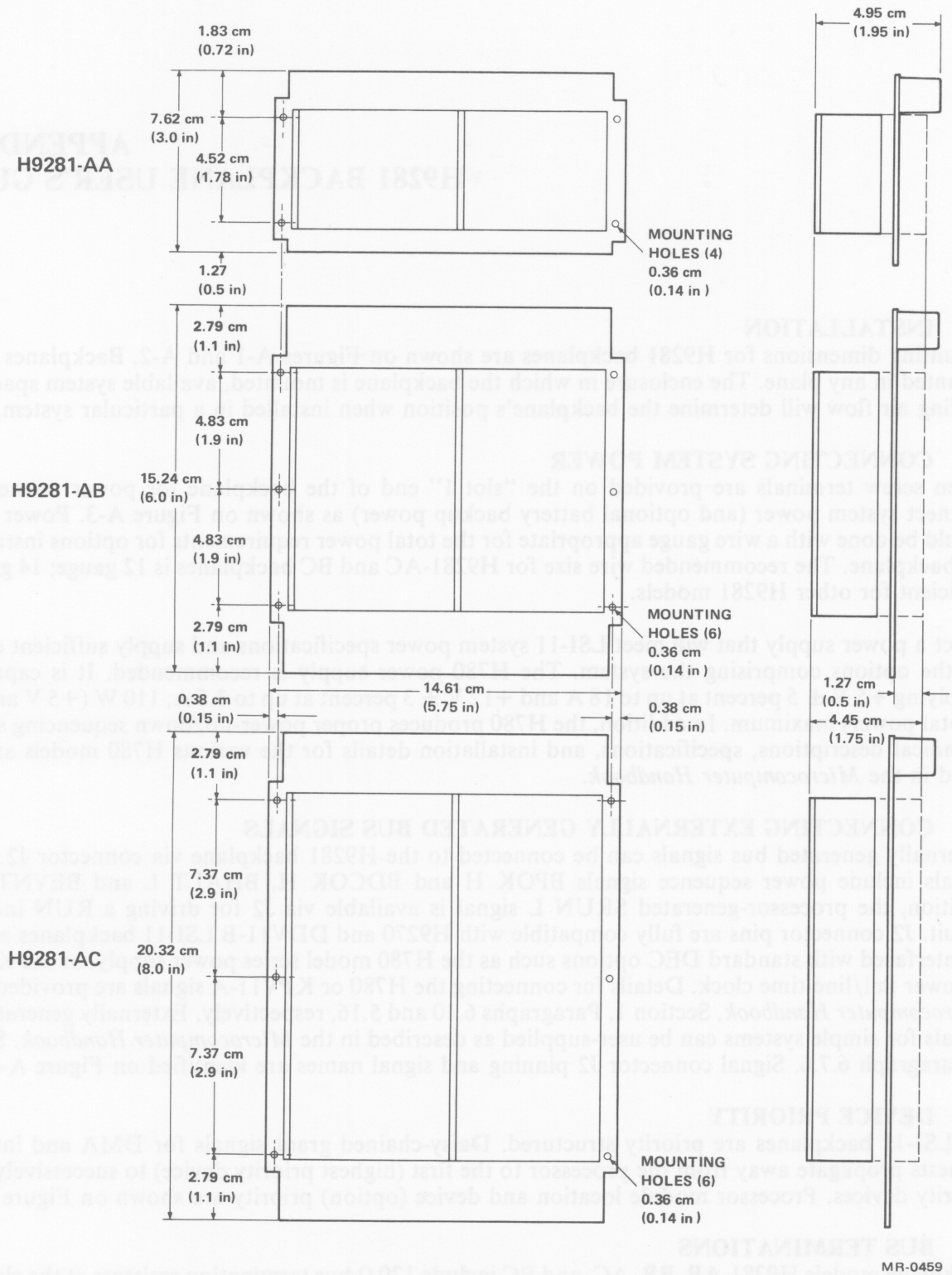


Figure A-1 H9281-AA, AB, AC Mounting Dimensions

MODEL	MOUNTING DIMENSION A	ASSEMBLY LENGTH B
H9281-BA	6.86 cm (2.7 in)	7.62 cm (3.0 in)
H9281-BB	11.94 cm (4.7 in)	15.24 cm (6.0 in)
H9281-BC	17.02 cm (6.7 in)	20.32 cm (8.0 in)

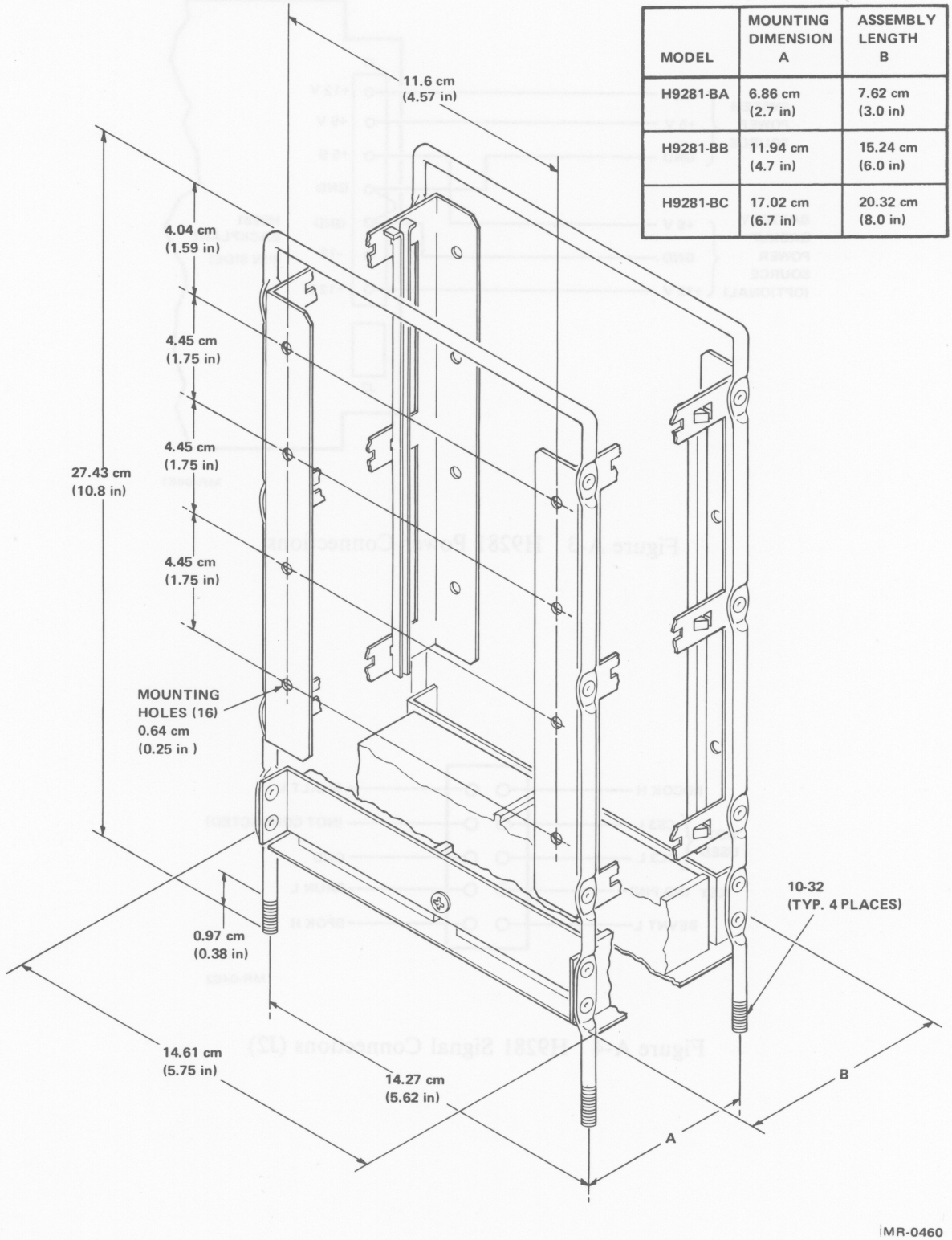


Figure A-2 H9281-BA, BB, BC Mounting Dimensions

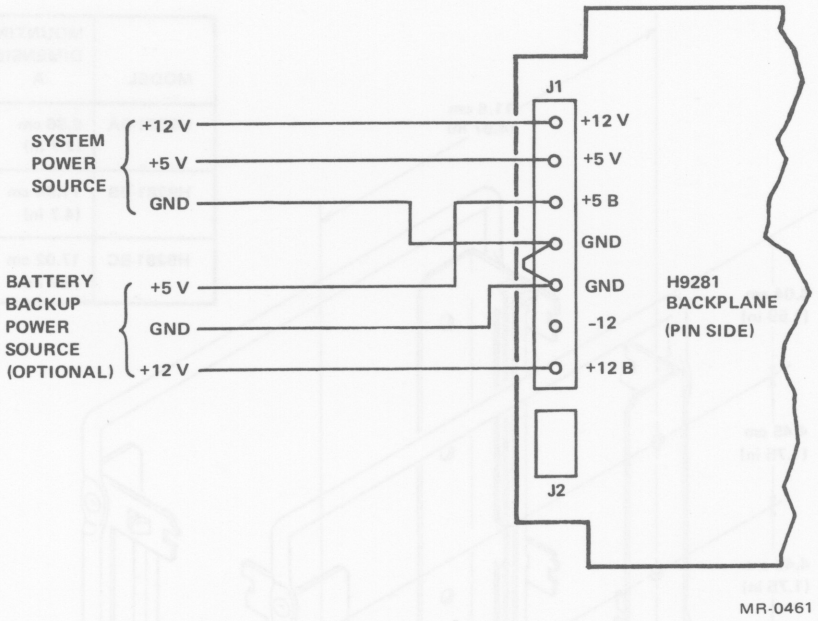


Figure A-3 H9281 Power Connections

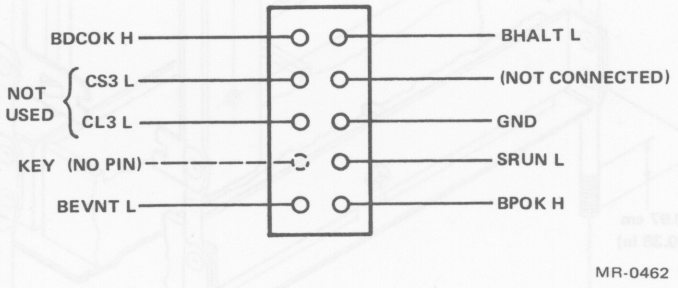


Figure A-4 H9281 Signal Connections (J2)

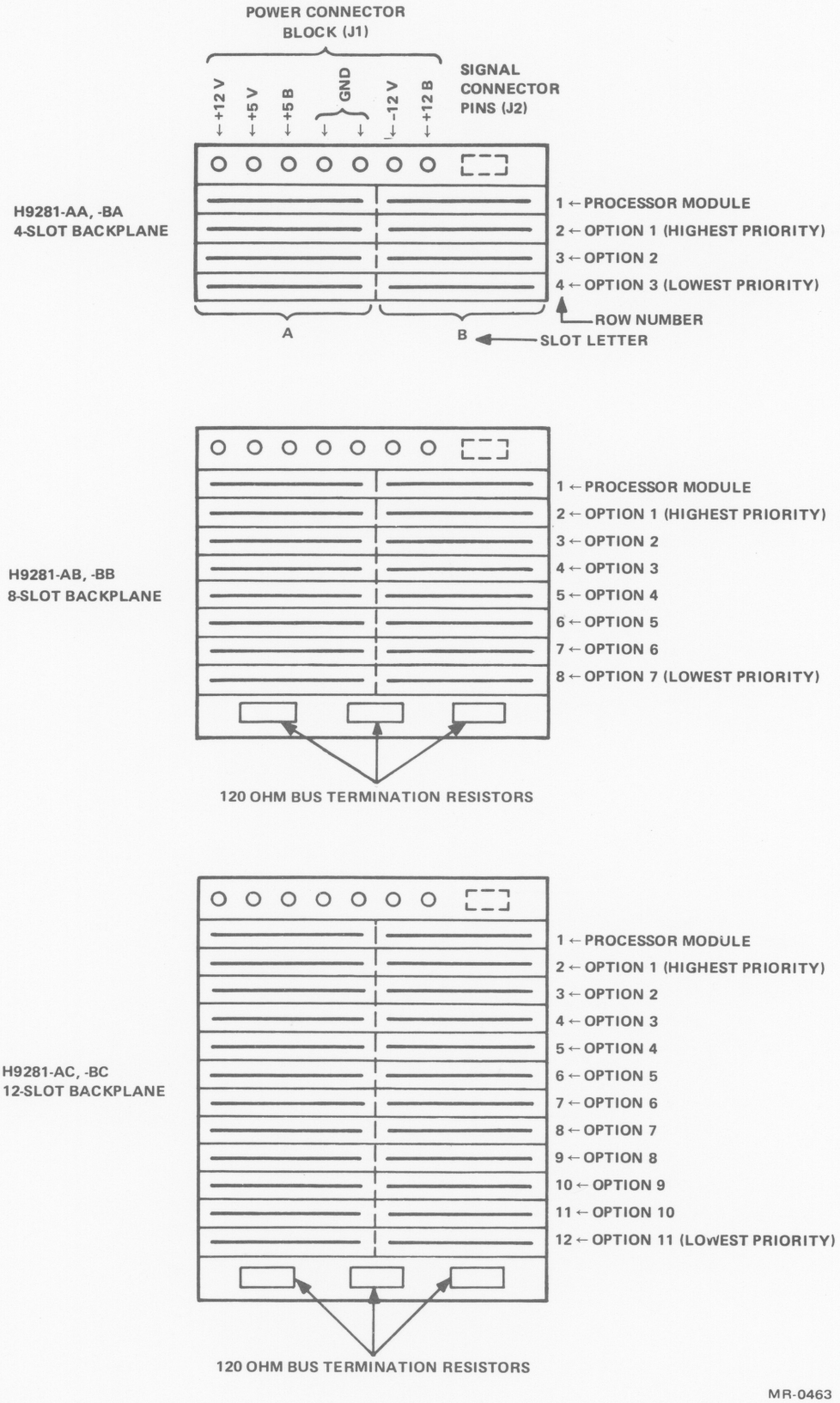


Figure A-5 H9281 Option and Connector Locations (Module Side)

M7270 LSI-11/2
MICROCOMPUTER MODULE
USER'S GUIDE
K-LSI11-UG-001

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